REMARKS

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R.§1.16 or §1.17 to Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at the telephone number listed below to discuss any matter regarding this application.

Attached hereto is a marked up version of the changes made to the specification by the current amendment. The attached page is captioned "**Clean Version of Replacement Paragraph.**"

Respectfully submitted,

Date: November 8, 2001

Sumeet Magoon
Registration No. 43,769

KENYON & KENYON
1500 K Street, N.W., Suite 700
Washington, D.C. 20005
Ph.: (202) 220-4200
Fax.: (202) 220-4201

Clean Version of Replacement Paragraph

Please replace the paragraph at page 2, beginning at line 6 with the following:

Typically, the merge occurs when the instruction is retired. For example, one prior art processor supports 8 and 16 bit operations. To merge an 8 or 16 bit result with the unchanged bits of a register, a prior art processor uses a Retired Register File (RRF). The RRF maintains copies of each of the eight physical registers of the x86. When an instruction is retired (which can occur well after the instruction was executed), the 8, 16, or 32 bit result of the instruction is transmitted to the RRF. Using its copy of the register in question, the RRF merges the result of the retired instruction along with the unchanged bits of the relevant source register. This provides a full 32 bit result with the unchanged bits intact to maintain architecture compatibility.